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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/602,914	06/25/2003	Chitoshi Ambe	108075-00110	1772

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EXAMINER	
PHAM, VAN T	

ART UNIT	PAPER NUMBER
2656	

DATE MAILED: 02/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/602,914	AMBE, CHITOSHI	
	Examiner	Art Unit	
	VAN T. PHAM	2656	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-18 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) 6-11 is/are allowed.

6)☒ Claim(s) 1-5 and 12-18 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 25 June 2003 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

1. Figures 1-3, and 6 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claims 1-4, 12-13 are rejected under 35 U.S.C. 102(a) as being anticipated by the admitted prior art.

Regarding claim 1, the admitted art on pages 1-4 of the specification and applicant's Figs. 1-6 discloses an apparatus for reading data from a disk, wherein the data is recorded in a data portion provided in each sector on the disk based on address information recorded in a header portion provided in that sector, the apparatus comprising: a read clock generating circuit (see Fig. 4) for generating a read clock signal based on rotational speed and recording density of the disk (see Figs. 1 and 4).

Regarding claim 2, discloses the apparatus according to claim 1, wherein the disk has a plurality of zones where data is recorded in those zones at different recording densities (see Fig. 6 and [0018]) and the read clock generating circuit includes an arithmetic operation circuit for computing a frequency of the read clock signal in accordance with the rotational speed of the disk and the recording density of each zone (see Figs. 1, 4 and 6).

Regarding claim 3, discloses the apparatus according to claim 1, wherein the disk has a plurality of zones where data is recorded in those zones at different recording densities, a frequency of the read clock signal differs zone by zone, and the read clock generating circuit includes a memory where a table of frequencies of a plurality of read clock signals associated with the plurality of zones is stored (see Figs. 1-3, 6).

Regarding claim 4, discloses the apparatus according to claim 1, further comprising an ID reading apparatus which operates in accordance with the read clock signal to read the address information and the data (see Fig. 5).

Regarding claim 12, discloses a method of reading data from a disk, the method comprising: generating a read clock signal based on rotational speed and recording density of the disk (see Fig. 4); reading address information from a header portion recorded in each sector of the disk in accordance with the read clock signal (see Fig. 3); and reading data recorded in a data portion of each sector based on the address information (see Figs. 3, 5).

Regarding claim 13, disclose the method according to claim 12, wherein said generating the read clock signal includes computation of a frequency of the read clock signal in accordance with the rotational speed and recording density of the disk (see Figs. 4, 6 and [0018]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 5, 14-18 is rejected under 35 U.S.C. 103(a) as being unpatentable over the admitted art as applied to claim 1 above, and further in view of Tsuyoshi et al. (US 4,949,325).

Regarding claim 5, the admitted art discloses the apparatus according to claim 1. However, the admitted art does not disclose a first delay circuit for generating from the read clock signal a first delay clock signal delayed by a predetermined phase from the read clock signal; and a second delay circuit for generating from the read clock signal a second delay clock signal delayed by the predetermined phase from the first delay clock signal.

Tsuyoshi see Fig. 7, discloses a first delay circuit for generating from the read clock signal a first delay clock signal delayed by a predetermined phase from the read clock signal; and a second delay circuit for generating from the read clock signal a second delay clock signal delayed by the predetermined phase from the first delay clock signal.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide a first delay and second delay in the admitted art as suggested by Tsuyoshi, the motivation being in order to extent that the phase difference detected between the reproduced phase correction pit signal and preformatted pit clock signal is minimal (see Tsuyoshi col. 2, lines 60-62).

Regarding claim 14, see rejection above of claim 5.

Regarding claim 15, the combination of the admitted art and Tsuyoshi, discloses the method according to claim 14, wherein said reading the address information includes reading of the address information at different timings in accordance with the plurality of delay clock signals (see Tsuyoshi Figs. 7 and col. 5, line 64- col. 6, line 36).

Regarding claim 16, the combination of the admitted art and Tsuyoshi, discloses the method according to claim 15, further comprising selecting a best read address and error detection result from the read address read at different timings and error detection results for the read addresses (see Tsuyoshi Fig. 7, element 21).

Regarding claim 17, the admitted art discloses a method of reading data from a disk, the method comprising: generating a read clock signal based on rotational speed and recording density of the disk. However, the admitted art does not disclose a plurality delay.

Tsuyoshi, see Fig. 7 and col. 1, lines 7-22, discloses generating a plurality of delay clock signals having different phases from one another from the read clock signal (see Fig. 7, clock signal S4); reading address information recorded in a header portion of each sector of the disk in accordance with the read clock signal (see Fig. 13); reading the address information in accordance with the plurality of delay clock signals (see Figs. 7 and 13); selecting the address information which has the greatest number of matches from the address information read at different timings (see Figs. 7, 13 and abstract); and reading the data based on the selected address information (see Fig. 15).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to provide plurality delay and selector in the admitted art as suggested by

Tsuyoshi, the motivation being in order to have the data pits are read out accurately in accordance with the clock signal (see Tsuyoshi col. 2, lines 60-62).

Regarding claim 18, the combination of the admitted art Tsuyoshi, discloses the method according to claim 17, wherein said generating the read clock signal includes computation of a frequency of the read clock signal in accordance with the rotational speed and recording density of the disk (see the admitted art Figs. 4, 6 and Tsuyoshi col. 5, lines 22-53).

Allowable Subject Matter

6. The following is an examiner's statement of reasons for allowance:

Claims 6-11 are allowable.

The admitted art discloses an apparatus for reading data recorded on a disk having sectors with each sector including a header portion having an address sync mark and address information and a data portion where the data is recorded, the apparatus comprising (see Fig. 3): a read clock generating circuit for generating a read clock signal based on a rotational speed and recording density of the disk (see Fig. 4); a first ID reading apparatus which operates in accordance with the read clock signal, the first ID reading apparatuses including: a first address sync mark detection circuit for detecting the address sync mark from data read from the header portion in accordance with the read clock signal and generating an address sync mark detection signal; a first ID reading circuit for reading address information from the read data in accordance with the address sync mark detection signal and the read clock signal (see Fig. 5); and a first ID decision circuit for generating a read address read from the address information and a decision result indicating whether the read address is normal in accordance with the read clock signal (see Fig. 5).

Tsuyoshi Figs. 7, 13 discloses a plurality of delay circuits for generating a plurality of delay clock signals having different phases from one another from the read clock signal; and a selector circuit which receives a plurality of read addresses and a plurality of decision results from the first reading apparatus and the plurality of second reading apparatuses and selects a best read address and decision result from there among.

None of the cited references discloses or suggests a plurality of second ID reading apparatuses which operate in accordance with the plurality of delay clock signals, the second ID reading apparatuses including: a second address sync mark detection circuit for detecting the address sync mark from data read from the header portion in accordance with an associated one of the plurality of delay clock signals and generating an address sync mark detection signal; a second ID reading circuit for reading address information from the read data in accordance with the address sync mark detection signal and the associated one of the plurality of delay clock signals; and a second ID decision circuit for generating a read address read from the address information and a decision result indicating whether the read address is normal in accordance with the associated one of the plurality of delay clock signals; Claims 7-10 fall with parent claim.

7. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Cited References

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The cited references relate to:

a. Method and associated apparatus and medium for optical recording and reproducing information (Tsuyoshi et al. US 4,949,325).

b. Signal decoding apparatus and method (Ogawa et al. US 5,070,492).

c. An optical recording/reproducing apparatus having drive means for rotating a recording medium (Kumagai et al. US 6,757,227).

d. Data reproducing apparatus and method (Tanaka US 5,848,040).

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to VAN T. PHAM whose telephone number is 571-272-7590. The examiner can normally be reached on Monday-Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wayne Young can be reached on 571-272-7582. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VY

WAYNE YOUNG
SUPERVISORY PATENT EXAMINER